Remarks

Claims 1-9, 11-18 and 20 are pending. Claims 10 and 19 are herein canceled without prejudice, and claims 1, 11 and 18 are herein amended. Claims 1 and 18 are amended to include the limitations of claim 10 and 19, respectively. Applicants submit that the amendments do not add new material to the current Application. No amendment made is related to the statutory requirements of patentability unless expressly stated herein. No amendment made is for the purpose of narrowing the scope of any claim, unless Applicants argue herein that such amendment is made to distinguish over a particular reference or combination of references.

Applicants respectfully submit claims 1-4, 8-9, 11-14,17-18, and 20 are patentable over Lee (U.S. 6,222,212) under 35 U.S.C. 102(e). Applicants submit that Lee fails to teach or suggest all limitations of independent claims 1, 11 and 18. More specifically, Lee fails to teach or suggest a packaging material formed on the fuse or the process of forming a packaging material on the fuse. Lee teaches forming two structures: 1) a semiconductor structure 801 having circuitry 811 and 812, and 2) a programmable semiconductor structure 802 having a programmable element 813. After forming each of the structures 801 and 802, they are joined to form an integrated circuit structure 800 with insulating layers 807, 804 and conductive layers 808, 805 formed therebetween. Lee's programmable element (fuse) 813 is formed in a semiconductor substrate 806 and, therefore, is in contact with the semiconductor substrate 806, the insulating layer 807 and the conductive layer 808. Lee is silent as to forming a packaging material and fails to teach forming a packaging material <u>on</u> the programmable element. Therefore, claims 1-4, 8-9, 11-14, 17-18 and 20 are not anticipated by Lee.

Furthermore, Applicants submit that claims 1-4, 8-9, 11-14, 17-18 and 20 are not obvious in view of Lee. Even if Lee was to form a packaging material over the integrated circuit structure 800, the packaging material would not be formed *<u>on</u>* the programmable interconnect element 813, although it may be formed *<u>over</u>* the programmable interconnect element 813. The packaging material cannot be formed on the programmable interconnect element 813, because the programmable interconnect element 813 is already in physical contact with the substrate 806, the insulating layer 807 and the conductive layer 808. Thus, there it is not possible to form anything *<u>on</u>* the programmable element 813 beyond what is taught and suggested by Lee.

In contrast, claims 1-4, 8-9, 11-14, 17-18 and 20 expressly recite "a packaging material formed on the fuse" or" forming a packaging material on the fuse." Since there is nothing in Lee to suggest these limitations, Applicants' claims 1-4, 8-9, 11-14, 17-18 and 20 are patentable over this reference in all respects.

Applicants respectfully submit that claim 5-7, 15 and 16 are patentable over Lee under 35 U.S.C. 103(a) for at least the same reasons that independent claims 1 and 11 are patentable over Lee under 35 U.S.C. 103(a), as discussed above.

Applicants would like to clarify that the date of publication of the reference AO should state "6/13/01", not "8/13/01". Prior to mailing the IDS, the typographical error was discovered. Applicants believe that the error was fixed and an IDS with the correct publication date was mailed to the USPTO when filing the present application. After the filing of the IDS it was discovered that the copy of the IDS in Applicants' folder incorrectly states 8/13/01. Applicants believe that in error the incorrect copy of the IDS form may have been placed in Applicant's folder. The IDS with the correct date should have been mailed to the USPTO. Applicants are unsure as to whether the USPTO's copy has the correct date. Please correct the publication date, if necessary. Thank you.

Believing to have responded to every issue raised by the Examiner in the communication mailed May 30, 2002, Applicants believe the present Application is currently in a condition of allowance. Applicants thank the Examiner for pointing out allowable subject matter, but herein earnestly solicit allowance of pending claims 1-15 and 27. Please contact Applicant's practitioner listed below if there are any issues.

Respectfully submitted,

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IN THE CLAIMS - VERSIONS WITH CHANGES SHOWN

Cancel claims 10 and 19 without prejudice.

1. (Amended) A semiconductor device, comprising:

a substrate having circuitry formed therein;

a passivation layer formed overlying at least a portion of the substrate; [and]

a fuse, which may be selectively open-circuited, formed overlying the passivation layer; and

a packaging material formed on the fuse.

11. A semiconductor device, comprising:

a substrate having a first circuit formed therein and a second circuit formed therein, wherein the first circuit has a first contact area and the second circuit has a second contact area;

a passivation layer formed overlying at least a portion of the substrate; [and]

a fuse, which may be selectively open-circuited, formed overlying the passivation layer, the fuse having a third contact area which is electrically coupled to the first contact area of the first circuit, and the fuse having a fourth contact area which is electrically coupled to the second contact area of the second circuit, wherein the first contact area of the first circuit and the second contact area of the second circuit are no longer electrically connected if the fuse is open-circuited; and

a packaging material formed on the fuse.

18. A method for forming a semiconductor device having a fuse, comprising:

providing a substrate;

forming a passivation layer overlying at least a portion of the substrate; [and]

forming the fuse overlying the passivation layer; and

forming a packaging material on the fuse.